IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A semiconductor nonvolatile storage device comprising:

a writing operation selecting circuit for selecting a temporary writing operation having a prescribed writing time for a memory cell transistor element and an additional writing operation for the memory cell transistor element; and

a writing time control circuit for controlling a [[the]] time length of the additional writing operation in accordance with the output signal of the writing operation selecting circuit.

2. (Original) A semiconductor nonvolatile storage device according to claim 1, wherein data written in the memory cell transistor element by the temporary writing operation is discriminated and the discriminated data is transferred to a write data holding circuit for the additional writing operation.

3. (Original) A semiconductor nonvolatile storage device according to claim 2, further including: a verifying operation control circuit for controlling a verifying operation for discriminating whether or not the data is normally written in the memory cell transistor element by the temporary writing operation; and a verifying circuit for performing the verifying operation in accordance with the output signal of the verifying operation control circuit.

4. (Original) A semiconductor nonvolatile storage device according to claim 2, further including a writing voltage setting circuit for controlling the set value of writing voltage in accordance with the output signal of the writing operation selecting circuit.

5. (Original) A semiconductor nonvolatile storage device according to claim 2, wherein an erasing operation is performed before the additional writing operation is performed.

6. (Original) A semiconductor nonvolatile storage device according to claim 2, further including: an erasing operation selecting circuit for selecting a primary erasing operation and a secondary erasing operation having a prescribed erasing time for the memory cell transistor element; and an erasing time control circuit for controlling an erasing time in accordance with the output signal of the erasing operation selecting circuit.

7. (Original) A semiconductor nonvolatile storage device according to claim 2, further including a reading operation selecting circuit capable of selecting a temporary reading operation after the temporary writing operation and a reading operation after the additional writing operation.

8. (Original) A semiconductor nonvolatile storage device according to claim 7, further including a reading voltage setting circuit to which the output signal of the reading operation selecting circuit is connected, and in which when the output signal indicates the temporary reading operation, the set value of word line voltage is set to temporary reading voltage.

9. (Original) A semiconductor nonvolatile storage device according to claim 7, further including a reference current setting circuit for allowing reference current as a decision reference of electric current to flow to the memory cell transistor element when read data is decided and controlling the set value of the reference current in accordance with the output signal of the reading operation selecting circuit.

10. (Original) A semiconductor nonvolatile storage device according to claim 2, wherein the write data holding circuit includes a latch provided at the rate of one for each bit line or several bit lines and a transfer gate for electrically separating the latch from the bit line, and further includes a bit line potential detecting circuit for detecting the voltage of the bit line and a

latch invert circuit for inverting the data of the latch in accordance with the output of the bit line potential detecting circuit.

11. (Original) A semiconductor nonvolatile storage device according to claim 2, further including an interrupt input circuit in which data is written for each writing block in a memory cell transistor array and when a writing instruction is inputted during performing the additional writing operation, the input of the writing instruction is permitted without performing the additional writing operation in other writing blocks after the additional writing operation is completed.

12. (Original) A semiconductor nonvolatile storage device according to claim 11, further including a ready/busy output circuit for informing about the inhibition of the input of write data while the additional writing operation is performed.

13. (Original) A semiconductor nonvolatile storage device according to claim 2, further including a writing flag for storing whether a writing state of data for each writing block in the memory cell transistor array indicates a state which is after a temporary writing state or after an additional writing state for each writing block.

14. (Original) A semiconductor nonvolatile storage device according to claim 13, wherein the additional writing operation is controlled to be performed for the writing block after the temporary writing operation on the basis of the information of the writing flag.

15. (Original) A semiconductor nonvolatile storage device according to claim 13, further including a word line voltage switching circuit for changing the reading voltage applied to a word line upon reading operation on the basis of the information of the writing flag.

16. (Original) A semiconductor nonvolatile storage device according to claim 2, further including a selector for selecting any of a plurality of semiconductor nonvolatile storage devices and controlling an operation.

17. (Original) A semiconductor nonvolatile storage device according to claim 16, wherein a ready/busy output circuit is provided for outputting an instruction for inhibiting the input of the write data to the selector while the additional writing operation is performed.

18. (Original) A semiconductor nonvolatile storage device according to claim 2, wherein an ECC circuit is further provided.

19. (Currently amended) A controlling method of writing a semiconductor nonvolatile storage device comprising:

a step of selecting a temporary writing operation having a prescribed writing time for a memory cell transistor element; and

a step of controlling a time length of an additional writing operation in accordance with the selection of the temporary writing operation.